REMARKS/ARGUMENTS

Claims 1-14 are pending in this application.

Initially, the Examiner's attention is drawn to the Preliminary Amendment filed November 17, 2005. It was not clear to the undersigned that the Examiner had considered that Amendment. All amendments made by the Preliminary Amendment are included in this Amendment as having been previously made.

Secondly, claims 1, 2, 9 and 10 have been amended by this Amendment to more particularly point out and distinctly claim the invention. These amendments have not been made for purposes of patentability and it is submitted that these claims are therefore entitled to the full range of equivalents under the Doctrine of Equivalents.

The Examiner has rejected claims 1 – 4 and 8 under U.S.C. § 102(b) as being anticipated by Makaran (U.S. Patent No. 6,630,803) ("Makaran"). The Examiner states that Makaran discloses an overcurrent protection circuit for a power switching transistor, which power switching transistor the Examiner notes is element 54 <MOSFET> of Fig. 29 (see p. 2, third paragraph, lines 1 – 2 of the Office Action). Applicant submits that the MOSFET 54 is not equivalent to the power switching transistor of claim 1 of the present application since the MOSFET 54 is not being protected by the "protection circuit", i.e., the snubber circuit 69 of Fig. 29, because it itself is the protection circuit. The power switching transistor that is being protected by the snubber circuit of Makaran is the switch S1 (Fig. 4 of Makaran), which is coupled in series with the motor coil (i.e., L1, R1, and E of Fig. 4). Therefore, MOSFET 54 corresponds to a "protection circuit," but it is not the circuit that is being protected and therefore cannot correspond to the "power switching transistor" of claim 1.

Further, the circuit of Makaran does not sense the "rate of change of voltage with respect to time at one of the main electrodes of the power switching transistor" as required by claim 1. The circuit of Makaran senses the absolute voltage level of the capacitor voltage across the capacitor C 56, which corresponds to the voltage level at one of the main electrodes of the power switching transistor, i.e., the switch S1 (see, e.g., col. 3, lines 62 – 66, and col. 11, lines 45 – 51). It is further noted that the operational amplifier (unlabeled) of Fig. 29 of Makaran (corresponding to op amp U1A 34 of Fig. 14) compares the voltage of the snubber capacitor C 56 (i.e., C1 of Fig. 14) to a reference voltage to control the switching of the MOSFET 54 (MOSFET Q1 50 of Fig. 14).

The Examiner also states the "protection switch" comprises elements transistors Q1, Q2, diode D3, and resistor Rp of Fig. 29 (p. 2, third paragraph, line 7 of the Office Action). However, the components Q1, Q2, D3, and Rp merely comprise a standard "totem pole" MOSFET driver (inverting type) for the snubber MOSFET 54 (col. 13, lines 6 – 10 of Makaran).

Therefore, claim 1 is patentably distinguishable over the Makaran reference and should be allowable. Claims 2, 3, 4, and 8 depend, either directly or indirectly, from claim 1, and are patentable for the same reasons as given above for claim 1.

The Examiner has rejected claims 9 – 11 and 14 under U.S.C. § 102(b) as being anticipated by Turvey et al. (U.S. Patent No. 6,759,835) ("Turvey"). The Examiner states that Turvey discloses an overcurrent protection circuit comprising an R-C circuit "for controlling the protection transistor (Fig. 4 element TR4) to remove a control signal to the control electrode of the power switching transistor to turn off the power switching transistor ... if the rate of change exceeds a predefined value" (p. 3, second paragraph, lines 7 – 10 of the Office Action). However, the R-C circuit of Turvey (i.e., R7 and C4 of

Fig. 5) does not control the protection transistor (i.e., TR4 of Fig. 4) to remove a control signal from the control electrode of the power switching transistor (i.e., TR1 of Fig. 5) as required by claim 9 of the present invention.

Indeed, Turvey simply states that the rate of change of voltage with time across the transistor TR1 is "controlled" using the components R7, D7, and C4 (col. 6, lines 18 – 20 of Turvey). Turvey does not teach the R-C circuit either controlling the protection switch or turning off the power switching transistor.

The R-C circuit of Turvey is directed to limiting both the voltage and the rate of change in voltage across the transistor TR1 (col. 2, line 66 – col. 3, line 15 of Turvey). See also col. 6, lines 4 – 10, which states that "the additional circuitry ... can be regarded as an inductive **load** protection circuit". In other words, the power switching transistor TR1 of Turvey is first turned off and then the rate of change in voltage (dv/dt) is limited to some predetermined level. In contrast, according to the present invention, the overcurrent protection circuit senses when the rate of change in voltage (dv/dt) exceeds a predetermined level, and then turns off the power switching transistor.

Accordingly, claim 9 is distinguishable over Turvey and should be allowable. Claims 10, 11, and 14 depend, either directly or indirectly, from claim 9, and are patentable over Turvey for the same reasons as given above for claim 9.

The Examiner has rejected claims 5, 6, 7 and 12 under U.S.C. § 103(a) as being unpatentable over Makaran in view of Turvey. For the reasons given above with respect to claim 1, claims 5, 6, 7, and 12 should be patentable over the combination of Makaran and Turvey.

The Examiner has rejected claim 13 under U.S.C. § 103(a) as being unpatentable over Turvey in view of Ohura et al (U.S. Patent No. 5,818,281) ("Ohura").

Ohura fails to provide the necessary teaching to enable one skilled in the art to produce the overcurrent protection circuit of the present invention. Therefore, claim 13 should be allowable in view of the above arguments presented for claims 9 – 12 and 14.

In view of the above, it is submitted that all claims in this application are now in condition for allowance, prompt notification of which is requested.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 12, 2006

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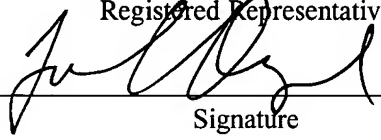

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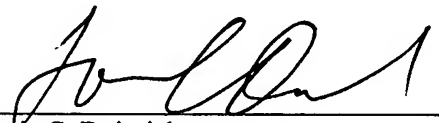
Respectfully submitted,



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